A1 cont'd

miniaturized since the number of pins to be mounted on one chip has been increased sharply following the recent acute requirement of development of semiconductor integrated circuits made finer.

Page 2, replace the paragraph, beginning on line 16, as follows:

A2

--The ESD protection apparatus of the present invention is to be installed between a pad of a semiconductor integrated circuit chip and an inner circuit of the semiconductor integrated circuit chip. The ESD protection apparatus is provided with a trigger element comprising a diode to be broken down by overvoltage applied to the pad and an ESD protection element comprising a longitudinal bipolar transistor also known in the art as a vertical bipolar transistor for discharging the accumulated electric charge of the pad by being electrically discharged attributed to the breakdown of the diode.--.

Page 3, replace the paragraph, beginning on line 9, bridging pages 3 and 4, as follows:

A3

--A first practical example of an ESD protection apparatus of the present invention is as follows. The pad is an input terminal or an output terminal. The trigger element comprises a first and a second diodes and a first and a second resistors. The ESD protection element comprises NPN type first and second longitudinal bipolar transistors. Regarding the first diode, the cathode is connected with the pad and the anode is connected with the base of the first longitudinal bipolar transistor. Regarding the second diode, the cathode is connected

with an electric power source terminal and the anode is connected with the base of the second longitudinal bipolar transistor. The first resistor is connected between the anode of the first diode and the ground terminal. The second resistor is connected between the anode of the second diode and the pad. Regarding the first longitudinal bipolar transistor, the collector is connected with the pad and the emitter is connected with the ground terminal. Regarding the second longitudinal bipolar transistor, the collector is connected with the electric power source terminal and the emitter is connected with the pad. Incidentally, at least either of a first diode, a first resistor and a first longitudinal bipolar transistor or a second diode, a second resistor and a second longitudinal bipolar transistor may be provided.--

Page 4, replace the paragraph, beginning on line 4, as follows:

--A second practical example of an ESD protection apparatus of the present invention is as follows. The pad is an electric power source terminal. The longitudinal bipolar transistor is NPN type. Regarding the diode, the cathode is connected with the pad and the anode is connected with the base of the longitudinal bipolar transistor. A resistor is connected between the anode of the diode and a ground terminal. Regarding the longitudinal bipolar transistor, the collector is connected with the pad and the emitter is connected with the ground terminal.--;

[replace the paragraph, beginning on line 13, as

follows:]

--An ESD protection apparatus of the present invention may has the following constitution. The trigger element comprises, as a diode to be broken down by overvoltage applied to the pad, a first longitudinal bipolar transistor whose collector and base work and which discharges the accumulated electric charge of the pad by being electrically discharged attributed to the breakdown of the diode. The ESD protection element comprises a second longitudinal bipolar transistor for discharging the accumulated electric charge of the pad by being electrically discharged attributed to the breakdown of the diode.--;

A4 cont

[replace the paragraph, beginning on line 23, bridging pages 4 and 5, as follows:]

--Practical examples of this case are as follows. The pad is an input terminal or an output terminal. The trigger element comprises an NPN type longitudinal bipolar transistor A and an NPN longitudinal bipolar transistor B working as the first longitudinal bipolar transistor and a first and a second resistors. The ESD protection element comprises an NPN type longitudinal bipolar transistor C and an NPN type longitudinal bipolar transistor D working as the second longitudinal bipolar transistor. Regarding the longitudinal bipolar transistors A, C, the collectors are connected with the pad and the bases are connected with each other and the emitters are connected with a ground terminal. The first resistor is connected between the bases of the longitudinal bipolar transistors A, C and the ground

terminal. Regarding the longitudinal bipolar transistors B, D, the collectors are connected with an electric power source terminal and the bases are connected with each other and the emitters are connected with the pad. The second resistor is connected between the bases of the longitudinal bipolar transistors B, D and the pad.--.

Page 5, replace the paragraph, beginning on line 13, as follows:

--The pad is an electric power source terminal. The first and second longitudinal bipolar transistors are NPN type and their collectors are connected with the pad and their bases are connected with each other and their emitters are connected with a ground terminal. A resistor is connected between the bases of the first and second longitudinal bipolar transistors and the ground terminal.--;

replace the paragraph, beginning on line 20, as follows:

--The conductive types P and N may be taken as reverse conductive types N and P, respectively. Even if the P and the N are reversed, the kind of a carrier alone is changed and naturally the same function can be realized. Incidentally, when the longitudinal bipolar transistor is taken as PNP type, the positions of the diode and the resistor are replaced with each other.--;

replace the paragraph, beginning on line 27, bridging pages 5 and 6, as follows:

--The diode may comprise a single diode or plural diodes connected in series, the overvoltage may be an forward voltage for the diode and the breakdown may be a substantial breakdown by being electrically discharged. The diode forward descending voltage is, compared with the breakdown voltage, hard to depend on high impurity concentration and a low voltage. Consequently, by selecting the number of diodes to be connected in series, a desired substantial breakdown voltage can be accurately set.--.

[Page 6, replace the paragraph, beginning on line 8, as follows:]

--In the ESD protection apparatus according to the invention, the collector layers of the above described first longitudinal bipolar transistor and the above described second longitudinal bipolar transistor may be as simultaneously formed.-

[replace the paragraph, beginning on line 13, as follows:]

--In the ESD protection apparatus according to the invention, the above described first longitudinal bipolar transistor and the above described second longitudinal bipolar transistor may have a common collector layer.--;

[replace the paragraph, beginning on line 17, bridging pages 6 and 7, as follows:]

--In the ESD protection apparatus according to the invention, the longitudinal bipolar transistor or the diode comprises all or some of: a first N^-type well formed on the P type silicon substrate surface; a second N^-type well adjacent to this

first N^-type well and formed on the P type silicon substrate surface; a second N^+layer formed on this second N^-type well surface; the P^-type well formed on the first N^-type well surface; the P^+layer and a first N^+layer formed on this P^-type well surface apart from each other; the insulation material installed between these P^+layer and the first N^+layer for preventing the electric connection with the P^+layer and the first N^+layer, wherein the second N^-type well and the P^-type well may be insulated by the insulation material for isolation and the P type silicon substrate and the P^-type well may be insulated by the insulation material for isolation. In this case, the conductive type P and N may be taken as the reverse conductive N and P, respectively.--

[Page 7, replace the paragraph, beginning on line 6, as follows:]

--In the ESD protection apparatus according to the invention, the P^+layer and the first and second N^+layers may be formed simultaneously with the P^+layer and the N^+layer of the CMOS transistor constituting the inner circuit.--;

[replace the paragraph, beginning on line 12, as follows:]

--In the ESD protection device according to the invention, a second N^-type well may be formed simultaneously with the N^-type well of the CMOS transistor constituting the inner circuit.--;

[replace the paragraph, beginning on line 17, as follows:]

--In the ESD protection device according to the invention, the insulation material may be a dummy gate or a mere insulation material formed simultaneously formed with the gate electrode and the gate insulation film of the CMOS transistor constituting the inner circuit. This dummy electrode or the insulation film may be formed in a ring shape on the silicon substrate surface.--;

Replace the paragraph, beginning on line 24, bridging pages 7 and 8, as follows:

--In the ESD protection apparatus according to the invention, the diode may comprise: the N^-type well formed on the P type silicon substrate surface; the P^+layer and the N^+layer formed on the N^-type well surface apart from each other; and the insulation material formed in the inside from the above described P type silicon substrate surface between these P^+layer and N^+layer. In this case, in the ESD protection apparatus according to the invention, the conductive type P and N may be the reverse conductive type N and P, respectively.--.

Page 8, replace the paragraph, beginning on line 5, as follows:

--In the ESD protection apparatus according to the invention, the diode comprises: the N^-type well formed on the P type silicon substrate surface; the P^-type well formed on this N^- type well surface; the P^+layer and the N^+layer formed on this P^- type well surface apart from each other; and the insulation material installed on the P type silicon substrate surface between

these P^+layer and N^+layer, wherein the P type silicon substrate and the P^-type well may be insulated by the insulation material for isolation. In this case, in the ESD protection apparatus according to the invention, the conductive type P and N may be taken as the reverse conductive type N and P, respectively.--;

[replace the paragraph, beginning on line 17, as follows:]

--An ESD protection apparatus of the present invention may further have the following constitution. The diode comprises a P^- type well formed on the surface of a silicon substrate, an N^+ type layer and a P^+ type layer formed on the P^- type well surface at an interval from each other, and a dummy gate electrode formed on the P^- type well via an insulation film and between the N^+ type layer and the P^+ type layer and connected with a ground terminal. In this case, the electric field between the N^+ layer and the dummy gate electrode is intensified, the ESD trigger at a lower voltage. Incidentally, the conductive type P and N may be the reverse conductive type N and P, respectively.---.

[Page 9, replace the paragraph, beginning on line 1, as follows:]

--A method for fabricating an ESD protection apparatus relevant to the present invention is a method for fabricating an ESD protection apparatus according to the invention and comprises the following steps. (1) A first step of simultaneously forming an N^- type well of a CMOS transistor composing the inner circuit and an N^- type well for connector connection to be connected with

the collector of the longitudinal bipolar transistor on a P type silicon substrate. (2) A second step of simultaneously forming a collector N^- type well to be a collector of the longitudinal bipolar transistor and an N^- type well of the diode on the P type silicon substrate. (3) A third step of simultaneously forming a P^- type layer to be a base in the collector N^- type well of the longitudinal bipolar transistor and a P^- type layer to be an anode in the N^- type well of the diode. (4) A fourth step of simultaneously forming an N^+ type layer in the P^- type well of the CMOS transistor, an N^+ type layer in the N^- type well for collector connection of the longitudinal bipolar transistor, an N^+ type layer to be an emitter in the P^- type layer of the longitudinal bipolar transistor, and an N^+ type layer to be a cathode in the P^- type layer of the diode. (5) A fifth step of simultaneously forming a P^+ type layer on the N^- type well of the CMOS transistor, a P^+ type layer on the P^- type layer of the longitudinal bipolar transistor, and a P^+ type layer on the P^- type layer of the diode. In this case, the method for fabricating the ESD protection apparatus according to the invention allows the anode and the cathode to be reversed.--.

Page 10, replace the paragraph, beginning on line 5, as follows:

--Further, the ESD protection apparatus fabrication method may further comprise a step of forming a dummy gate electrode simultaneously with a gate electrode of the CMOS transistor in the region where the collector N^- type well of the

longitudinal bipolar transistor and N^- type well of the diode are formed in the second step (2). Incidentally, the dummy gate electrode is to prevent connection between the N^+ type layers of the longitudinal bipolar transistor and the diode formed in the step (4) and the P^+ type layers of the longitudinal bipolar transistor and the diode formed in the step (5) in the subsequent steps. Alternatively, the ESD protection apparatus fabrication method may further comprise a step of forming an insulation layer which prevents connection between the N^+ type layers of the longitudinal bipolar transistor and the diode formed in the step (4) and the P^+ type layers of the longitudinal bipolar transistor and the diode formed in the step (5) in the subsequent steps. In the method for fabricating the ESD protection apparatus relevant to the present invention also, the conductive type P and N may be the reverse type N and P, respectively.--.

Page 12, replace the paragraph, beginning on line 21, as follows:

--FIG. 17 is a plan view of the ESD protection apparatus in Fig 16;--.

Page 14, replace the paragraph, beginning on line 18, bridging pages 14 and 15, as follows:

-- The ESD protection apparatus of this embodiment is installed between an input terminal (an input pad) 6 of a semiconductor integrated circuit chip and a CMOS transistor 100 and comprises a trigger element 310 comprising diodes 311, 312 which are broken down by overvoltage applied to the input terminal

6 and an ESD protection element 210 comprising longitudinal bipolar transistors 211, 212 for discharging the accumulated electric charge of the input terminal 6 by being electrically discharged owing to the breakdown of the diodes 311, 312. Incidentally, FIG. 2 and FIG. 3 show only the longitudinal bipolar transistor 211 as some of ESD protection element 210 and only the diode 311 as some of the trigger element 310.--.

Page 15, replace the paragraph, beginning on line 3, as follows:

--The CMOS transistor 100 is a CMOS inverter comprising an NMOS transistor 101 and a PMOS transistor 102. Regarding the diode 311, the cathode is connected with the input terminal 6 and the anode is connected with the base of the longitudinal bipolar transistor 211. Regarding the diode 312, the cathode is connected with an electric power terminal 7 and the anode is connected with the base of the longitudinal bipolar transistor 212. A resistor 313 is connected with the anode of the diode 311 and a ground terminal 8. A resistor 314 is connected between the anode of the diode 312 and the input terminal 6. The longitudinal bipolar transistors 211, 212 are both NPN type. Regarding the longitudinal bipolar transistor 211, the collector is connected with the input terminal 6 and the emitter is connected with the ground terminal 8. Regarding the longitudinal bipolar transistor 212, the collector is connected with electric power terminal 7 and the emitter is connected with the input terminal 6. The resistors 313, 314 are made of a single crystal silicon, a polysilicon, a

metal or the like formed in the same semiconductor integrated circuit chip.--

[replace the paragraph, beginning on line 21, bridging pages 15 and 16, as follows:]

--Since today it has swiftly been promoted to make the gate insulation film of a CMOS transistor thinner, it is required for the ESD protection apparatus 210 to work at a lower voltage than that which the gate insulation film of the CMOS transistor 100 is broken. In this embodiment, the base potential of the longitudinal bipolar transistors 211, 212 is increased by voltage decreased at the time when the trigger current, which is the breakdown current of the diodes 311, 312, flows in the resistors 313, 314 to turn on longitudinal bipolar transistors 211, 212. Consequently, the large quantity of the electric charge attributed to the static electricity accumulated in the input terminal 6 is released in the longitudinal direction of the silicon substrate. As a result, electric current concentration can be prevented and a high ESD withstand level can be obtained.--.

Page 20, replace the paragraph, beginning on line 26, bridging pages 20 and 21, as follows:

--The ESD protection apparatus of this embodiment is installed between an electric power terminal (an electric power pad) 7 of a semiconductor integrated circuit chip and an inner circuit 103 and comprises a trigger element 315 comprising a diode 316 to be broken down by overvoltage applied to the electric power terminal 7 and an ESD protection element 213 comprising a

longitudinal bipolar transistor 214 for discharging the accumulated electric charge of the electric power terminal 7 by being electrically discharged owing to the breakdown of the diode 316.--.

Page 23, replace the paragraph, beginning on line 13, as follows:

--The ESD protection apparatus of this embodiment is installed between an electric power terminal (an electric power pad) 7 of a semiconductor integrated circuit chip and an inner circuit 103 and comprises a trigger element 400 comprising a diode 402 to be broken down by overvoltage applied to the electric power terminal 7 and an ESD protection element 200 comprising a longitudinal bipolar transistor 201 for discharging the accumulated electric charge of the electric power terminal 7 by being electrically discharged owing to the breakdown of the diode 402.--.

Page 27, replace the paragraph, beginning on line 27, bridging pages 27 and 28, as follows:

--The ESD protection apparatus of the present embodiment is installed between an input terminal (an input pad) 6 of a semiconductor integrated circuit chip and a CMOS transistor 100 and comprises a trigger element 510 comprising diodes 511, 512 which are broken down by overvoltage applied to the input terminal 6 and an ESD protection element 210 comprising longitudinal bipolar transistors 211, 212 for discharging the accumulated electric charge of the input terminal 6 by being electrically

A10 cont'd

discharged owing to the breakdown of the diodes 511, 512. The diodes 511, 512 are a plurality of diodes connected in series, and the overvoltage is a forward voltage for the diodes 511, 512 and the breakdown is a substantial breakdown by being electrically discharged. Incidentally, the diodes 511, 512 are illustrated in FIG. 26 as four diodes connected in series, but in FIG. 27 simplified and illustrated as two diodes connected in series for convenience's sake.--.

Page 30, replace the paragraph, beginning on line 9, as follows:

A11

--If a trigger voltage of one stage portion of the diode is taken as Vf (about 0.6V), the trigger voltage Vf of the diodes of four stages connected in series is Vf x 4 = about 2.4V. When a surge of the ESD is applied to the pad and exceeds 2.4V, the forward series connection diodes are electrically discharged and inject the electric current into the base of the longitudinal bipolar transistor. By this trigger electric current, the longitudinal bipolar transistor which is a protection element of a high driving force starts operation, thereby discharging a charge of the ESD.--.

Page 31, replace the paragraph, beginning on line 6, as follows:

A12

--The ESD protection apparatus of the present embodiment comprises a trigger element 515 comprising a diode 516 which is provided between the power source terminal 7 and the inner circuit 103 of the semiconductor integrated circuit and is broken down by

overvoltage applied to an electric power source terminal 7, and an ESD protection element 213 comprising the longitudinal bipolar transistor 214 for discharging the accumulated electric charge of the electric power source terminal 7 by being electrically discharged owing to the breakdown of the diode 516. The diode 516 is a plurality of diodes connected in series, and the overvoltage is a forward voltage for the diode 516 and the breakdown is a substantial breakdown by being electrically discharged.--.

Page 32, replace the paragraph, beginning on line 27, bridging pages 32 and 33, as follows:

--In the diode comprising the P^+layers 2/the N well 5 as shown in FIG. 27, since a parasitic longitudinal bipolar transistor comprising the P^+ 2 layer/the N well 5/a P substrate 51 is formed, the electric current flowing into the P substrate 51 is generated. For this reason, the electric current to be supplied to the longitudinal bipolar transistor which is a protection element is reduced. However, in the present embodiment, since an N well 527 formed simultaneously with a collector layer 17 of an ESD protection element 210 exists, the diode comprising the N^+layer 521/the P^-layer 526 can prevent the electric current flowing in a longitudinal direction (depth direction of substrate), and therefore the electric current can be supplied to the base of the ESD protection element 210 with high efficiency (refer to FIG. 32). Consequently, according to the present embodiment, since a trigger electric current can be supplied to a base of the longitudinal bipolar transistor with high efficiency,